19-2860; Rev 0; 4/03

High-Speed, Dual-Phase Gate Driver for Multiphase, Step-Down Converters

General Description

The MAX8523 dual-phase gate driver, along with the MAX8524*/MAX8525 multiphase controllers, provides flexible 2- to 8-phase CPU core-voltage supplies. The 0.5Ω/0.95Ω driver resistance allows up to 30A output current per phase.

Each MOSFET driver in the MAX8523 is capable of driving 3000pF capacitive loads with only 15ns propagation delay and 11ns typical rise and fall times, allowing operations up to 1.2MHz per phase. Adaptive dead time controls low-side MOSFET turn-on, and user-programmable dead time controls high-side MOSFET turn-on. This maximizes converter efficiency while allowing operation with a variety of MOSFETs and controller ICs. An undervoltage lockout (UVLO) circuit allows proper power-on sequencing. PWM_ signal inputs are both TTL and CMOS compatible.

The MAX8523 is available in a space-saving 16-pin QSOP package, and specified for -40°C to +85°C operation.

Applications

Core Voltage Supplies for Pentium™ IV Microprocessors

Servers and Workstations

Desktop Computers

Voltage Regulator Modules (VRMs)

DC-to-DC Regulator Modules

Switches, Routers, and Storage

Features

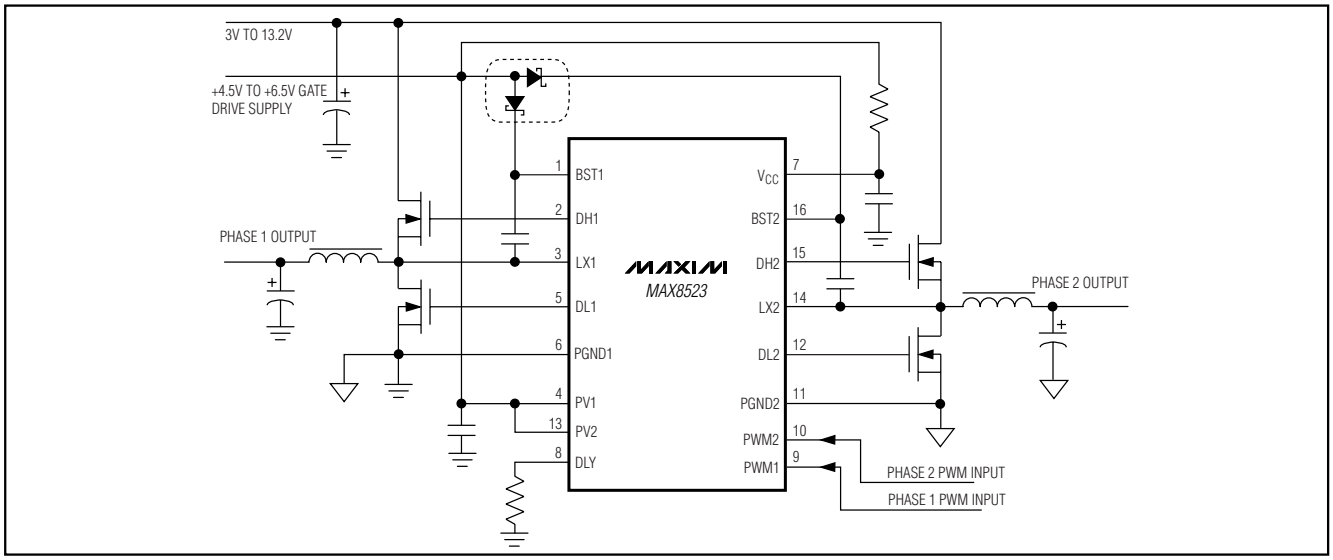
- **6A Peak Gate-Drive Current**
- **Up to 1.2MHz Operation**
- **Up to 6.5V Gate-Drive Voltage**
- **0.5Ω/0.95Ω Low-Side Drivers**
- **Capable of 30A Output per Phase**
- **Adaptive Shoot-Through Protection**
- **User-Programmable Delay Time**
- **TTL and CMOS Input Compatible**
- **UVLO for Proper Sequencing**
- **Flexible 2- to 8-Phase Implementation with MAX8524 and MAX8525**
- **Space-Saving (4.9mm × 6mm) 16-Pin QSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8523EEE	-40°C to +85°C	16 QSOP

**Future product. Contact factory for availability.*

Typical Operating Circuit



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High-Speed, Dual-Phase Gate Driver for Multiphase, Step-Down Converters

ABSOLUTE MAXIMUM RATINGS

BST_ to PGND_ .....-0.3V to +26V
LX_ to PGND_.....-1V to +14V
DH_ to PGND_.....-0.3V to (BST_ + 0.3V)
DH_ to LX_.....-0.3V to +7V
BST_ to LX_ .....-0.3V to +7V
DL_ to PGND_.....-0.3V to (PV_ + 0.3V)
PV_ to PGND_ .....-0.3V to +7V
PGND2 to PGND1 .....-0.3V to +0.3V
V_{CC} to PGND1.....-0.3V to +7V
DLY to PGND1.....-0.3V to (V_{CC} + 0.3V)
PWM_ to PGND1 .....-0.3V to (PV2 + 0.3V)
V_{CC} to PV1_.....-7V to +0.3V
DH_, DL_ Continuous Current .....±200mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{VCC} = V_{PV1} = V_{PV2} = V_{BST1} = V_{BST2} = V_{DLY} = 5V, V_{PGND1} = V_{PGND2} = V_{LX1} = V_{LX2} = 0V; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
UNDERVOLTAGE PROTECTION					
Supply Voltage Range		4.5		6.5	V
UVLO	V_{CC} rising	3.25	3.5	3.8	V
	V_{CC} falling	3.0		3.5	
I_{VCC}	DLY = V_{CC}		50	100	µA
	Dynamic, R_{DLY} = 50kΩ		0.5	1	mA
$I_{PV\_}$	PWM_ = GND		1	10	µA
	PWM_ = V_{CC}		1.2	2	mA
$I_{BST\_}$	PWM_ = GND		0.1	10	µA
	PWM_ = V_{CC}		1.2	2	mA
I_{BST1} + I_{PV1} + I_{BST2} + I_{PV2}	250kHz		4	8	mA
DRIVER SPECIFICATIONS					
DH_ Driver Resistance	PWM_ = PGND1, V_{BST} = 4.5V		0.65	1.2	Ω
	PWM_ = V_{CC}, $V_{BST\_}$ = 4.5V		0.8	1.35	
DL_ Driver Resistance	PWM_ = PGND1, $V_{PV\_}$ = 4.5V		0.95	1.6	Ω
	PWM_ = V_{CC}, V_{PV} = 4.5V		0.5	0.9	
DH_ Rise Time	PWM_ = V_{CC}, V_{BST} = 5V, 3nF load		11		ns
DH_ Fall Time	PWM_ = PGND1, V_{BST} = 5V, 3nF load		9.5		ns
DL_ Rise Time	PWM_ = V_{CC}, V_{PV} = 5V, 3nF load		8.5		ns
DL_ Fall Time	PWM_ = PGND1, V_{PV} = 5V, 3nF load		6.5		ns
DH_ Propagation Delay	PWM_falling, V_{BST} = 5V		15		ns
DL_ Propagation Delay	PWM_rising, V_{BST} = 5V		8		ns
PWM_ INPUT					
Input Current	$V_{PWM\_}$ = 0V or 6.5V		0.01	1	µA
Input Voltage High		2.5			V
Input Voltage Low				0.8	V

ELECTRICAL CHARACTERISTICS

(V_{VCC} = V_{PV1} = V_{PV2} = V_{BST1} = V_{BST2} = 5V, V_{PGND1} = V_{PGND2} = V_{LX1} = V_{LX2} = 0V; **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

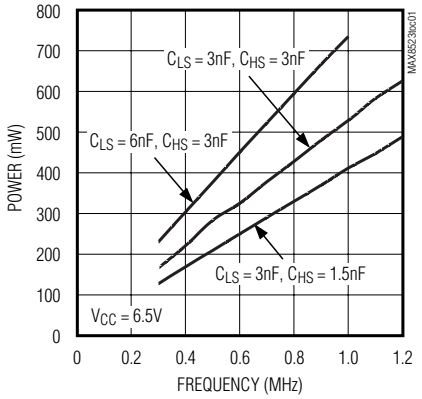
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
UNDERVOLTAGE PROTECTION					
Supply Voltage Range		4.5		6.5	V
UVLO	V_{CC} rising	3.25		3.8	V
	V_{CC} falling	3.0		3.5	
I_{VCC}	DLY = V_{CC}			100	µA
	Dynamic, R_{DLY} = 50kΩ			1	mA
$I_{PV\_}$	PWM_ = GND			10	µA
	PWM_ = V_{CC}			2	mA
$I_{BST\_}$	PWM_ = GND			10	µA
	PWM_ = V_{CC}			2	mA
I_{BST1} + I_{PV1} + I_{BST2} + I_{PV2}	250kHz			8	mA
DRIVER SPECIFICATIONS					
DH_ Driver Resistance	PWM_ = PGND1, $V_{BST\_}$ = 4.5V			1.2	Ω
	PWM_ = V_{CC}, $V_{BST\_}$ = 4.5V			1.35	
DL_ Driver Resistance	PWM_ = PGND1, $V_{PV\_}$ = 4.5V			1.6	Ω
	PWM_ = V_{CC}, $V_{PV\_}$ = 4.5V			0.9	
PWM_ INPUT					
Input Current	$V_{PWM\_}$ = 0V or 6.5V			1	µA
Input Voltage High		2.5			V
Input Voltage Low				0.8	V

Note 1: Specifications at -40°C guaranteed by design.

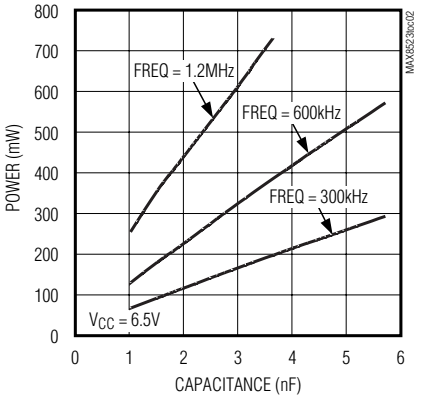
Typical Operating Characteristics

(PV1 = PV2 = V_{CC} = V_{DLY} = 5V, 3nF capacitive load, T_A = +25°C, unless otherwise noted.)

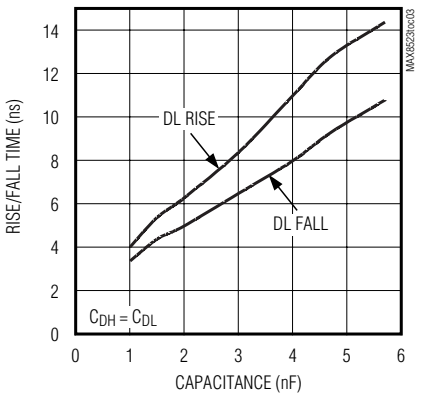
POWER DISSIPATION vs. SWITCHING FREQUENCY (BOTH DRIVERS SWITCHING)



POWER DISSIPATION vs. CAPACITIVE LOAD (BOTH DRIVERS SWITCHING)



DL RISE AND FALL vs. CAPACITIVE LOAD

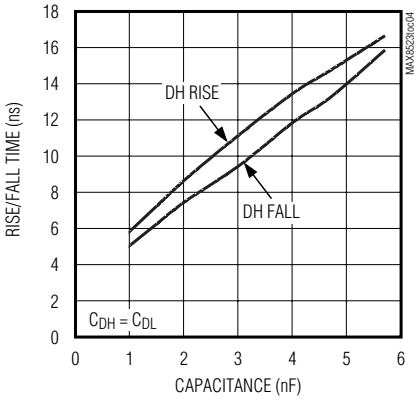


High-Speed, Dual-Phase Gate Driver for Multiphase, Step-Down Converters

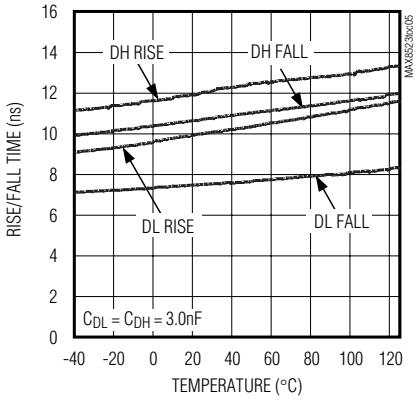
Typical Operating Characteristics (continued)

(PV1 = PV2 = V_{CC} = V_{DLY} = 5V, 3nF capacitive load, T_A = +25°C, unless otherwise noted.)

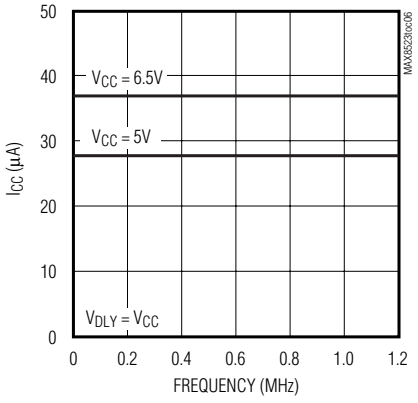
DH RISE AND FALL vs. CAPACITIVE LOAD



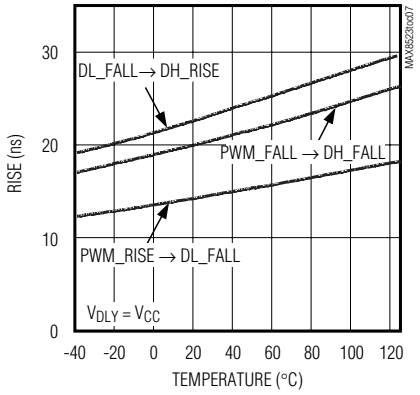
DH AND DL RISE AND FALL TIMES vs. TEMPERATURE



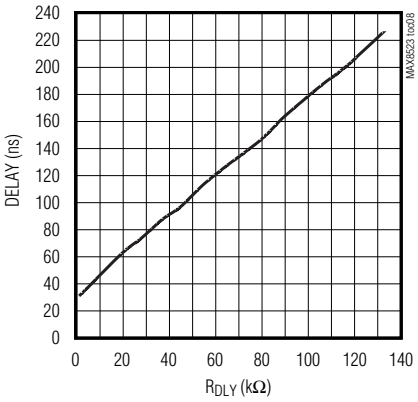
V_{CC} SUPPLY CURRENT vs. SWITCHING FREQUENCY



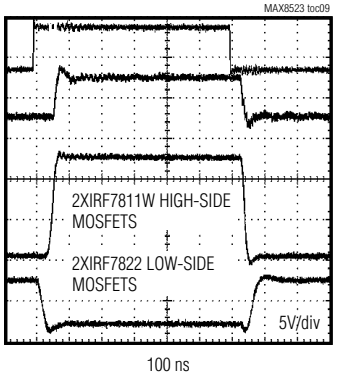
PROPAGATION DELAY vs. TEMPERATURE



PROGRAMMABLE DELAY vs. R_{DLY}



TYPICAL SWITCHING WAVEFORMS



Pin Description

PIN	NAME	FUNCTION
1	BST1	Boost Flying Capacitor Connection, Phase 1. Connect a 0.22µF or higher ceramic capacitor between BST1 and LX1.
2	DH1	High-Side Gate-Driver Output, Phase 1
3	LX1	Switching Node (Inductor) Connection, Phase 1
4	PV1	Gate-Drive Supply for DL1. Bypass to PGND1 with a 2.2µF or higher capacitor. Connect PV1 and PV2 together.
5	DL1	Low-Side Gate-Driver Output, Phase 1
6	PGND1	Power Ground for DL1. Connect PGND1 and PGND2 together. Internal analog ground is connected to PGND1.
7	V_{CC}	Supply Voltage. Bypass V_{CC} to PGND1 with a 0.1µF (min) capacitor.
8	DLY	Connect a resistor from DLY to PGND1 to set dead time between DL_ falling and DH_ rising. Connect to V_{CC} for default 20ns delay.
9	PWM1	Phase 1 PWM Logic Input. DH1 is high when PWM1 is high; DL1 is high when PWM1 is low.
10	PWM2	Phase 2 PWM Logic Input. DH2 is high when PWM2 is high; DL2 is high when PWM2 is low.
11	PGND2	Power Ground for DL2
12	DL2	Low-Side Gate-Driver Output, Phase 2
13	PV2	Gate-Drive Supply for DL2. Bypass to PGND2 with a 2.2µF or higher capacitor. Connect PV1 and PV2 together.
14	LX2	Switching Node (Inductor) Connection, Phase 2
15	DH2	High-Side Gate-Driver Output, Phase 2
16	BST2	Boost Flying Capacitor Connection, Phase 2. Connect a 0.22µF or higher ceramic capacitor between BST2 and LX2.

Detailed Description

The MAX8523 dual-phase gate driver, along with the MAX8524/MAX8525 multiphase controllers, provides flexible 2- to 8-phase CPU core-voltage supplies. The 0.5Ω/0.95Ω driver resistance allows up to 30A output current per phase.

Each MOSFET driver in the MAX8523 is capable of driving 3000pF capacitive loads with only 15ns propagation delay and 11ns typical rise and fall times, allowing operations up to 1.2MHz per phase. Adaptive dead time controls low-side MOSFET turn-on, and user-programmable dead time controls high-side MOSFET turn-on. This maximizes converter efficiency, while allowing operation with a variety of MOSFETs and PWM controller ICs. A UVLO circuit allows proper power-on sequencing. PWM_ signal inputs are both TTL and CMOS compatible.

Principle of Operation

MOSFET Gate Drivers (DH_, DL_)

The high-side drivers (DH_) have typical 0.8Ω sourcing resistance and 0.65Ω sinking resistance, resulting in 6A peak sourcing current and 7A peak sinking current with 5V supply voltage. The low-side drivers (DL_) have typical 0.95Ω sourcing resistance and 0.5Ω sinking resistance, yielding 5A peak sourcing current and 10A peak sinking current. This reduces switching losses, making the MAX8523 ideal for both high-frequency and high-output-current applications.

Shoot-Through Protection

Adaptive shoot-through protection is incorporated for the switching transition after the high-side MOSFET is turned off and before the low-side MOSFET is turned on. The low-side driver is turned on only when the LX voltage falls below 1.8V. Furthermore, the delay time between the low-side MOSFET turn-off and high-side MOSFET turn-on can be adjusted by selecting the value of R2 (see the *R_{DLY} Selection* section).

High-Speed, Dual-Phase Gate Driver for Multiphase, Step-Down Converters

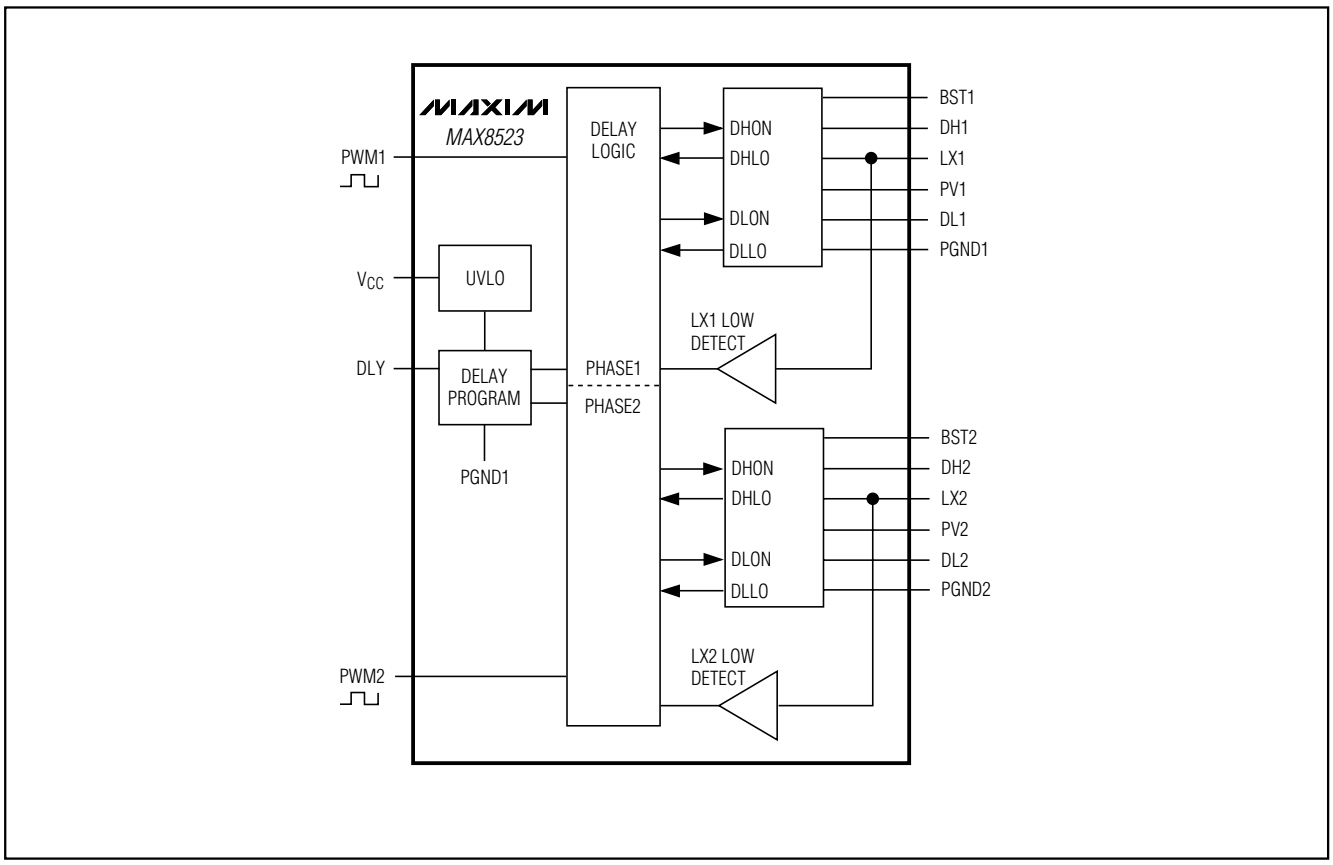


Figure 1. MAX8523 Functional Diagram

Undervoltage Lockout (UVLO)

When V_{CC} is below the UVLO threshold (3.5V typ), DH_ and DL_ are held low. Once V_{CC} is above the UVLO threshold and PWM_ is low, DL_ is kept high and DH_ is kept low. This prevents output from rising before a valid PWM signal is applied.

VCC Decoupling

V_{CC} provides the supply voltage for the internal logical circuit. To avoid malfunctions due to the switching noise on the DH_, DL_, and LX_ pins, RC decoupling is recommended for the V_{CC} pin. Place a 10Ω resistor (R1) from the supply voltage to the V_{CC} pin and a 0.1µF (C7) capacitor from the V_{CC} pin to PGND1.

Boost Capacitor Selection

The MAX8523 uses a bootstrap circuit to generate the floating supply voltages for the high-side drivers (DH_). The selected high-side MOSFET determines appropriate boost capacitance values, according to the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}}$$

where Q_{GATE} is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET drive. Choose ΔV_{BST} = 0.1V to 0.2V when determining the C_{BST}. Low-ESR ceramic capacitors should be used for C_3 and C_4.

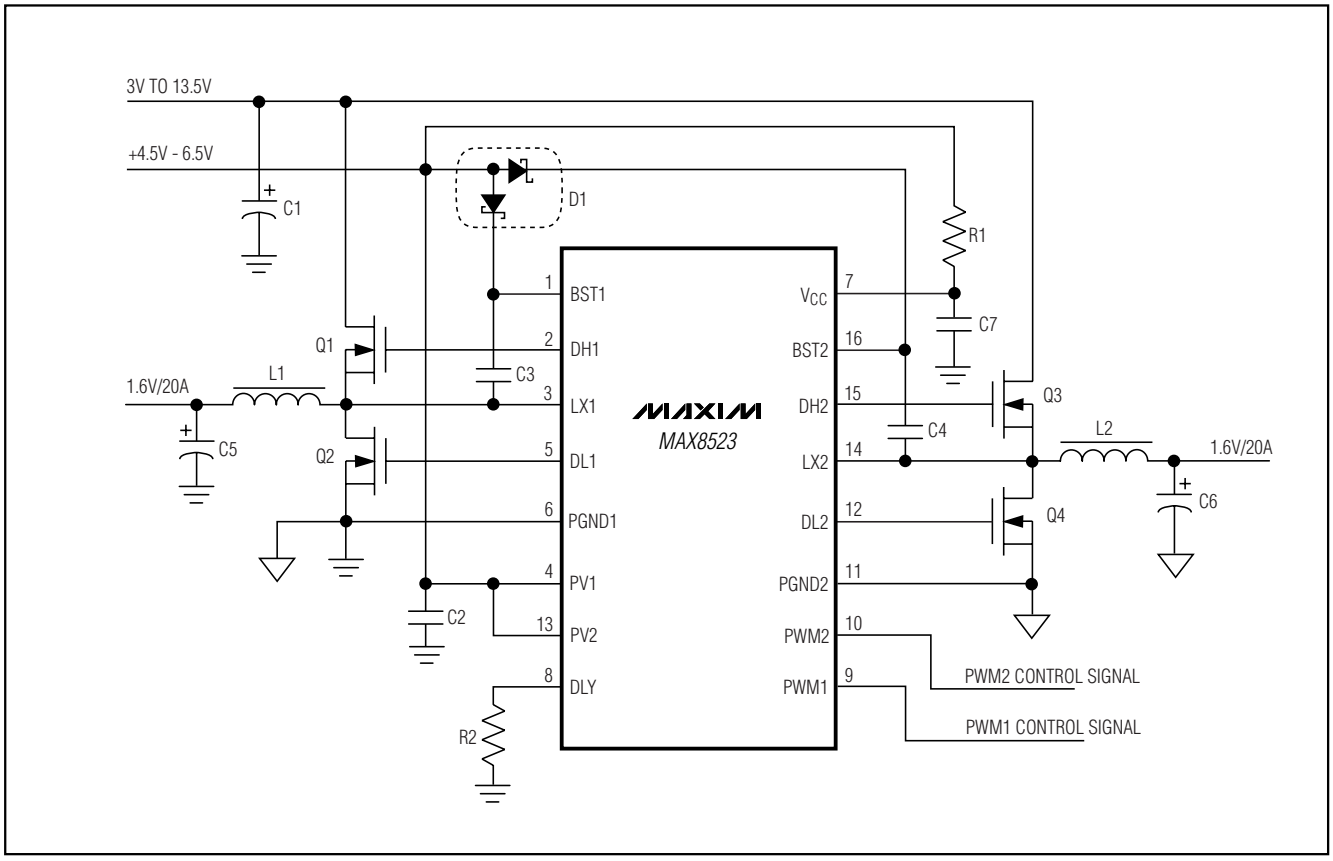


Figure 2. Typical Application Circuit

PV_ Decoupling

PV_ provides the supply voltages for the low-side drivers (DL_). The decoupling capacitors at PV_ also charge the BST capacitors during the time period when DL_ is high. Therefore, the decoupling capacitor C2 for PV_ should be large enough to minimize the ripple voltage during switching transitions. C2 should be chosen according to the following equation:

$$C2 = 10 \times C_{BST}$$

RDLY Selection

Connect DLY to V_{CC} for the default delay time, typically 20ns. Add a delay resistor, R_{DLY}, between DLY and PGND1 to increase the delay between the low-side MOSFET drive turn-off and the high-side MOSFET turn-on. See the *Typical Operating Characteristics* to select R_{DLY}.

Avoiding dV/dt-Induced Low-Side MOSFET Turn-On

At high input voltages, fast turn-on of the high-side MOSFET could momentarily turn on the low-side MOSFET due to the high dV/dt appearing at the drain of the low-side MOSFET. The high dV/dt causes a current flow through the Miller capacitance (C_{RSS}) and the input capacitance (C_{ISS}) of the low-side MOSFET. Improper selection of the low-side MOSFET that has a high ratio of C_{RSS}/C_{ISS} makes the problem more severe. To avoid the problem, give special attention to the ratio of C_{RSS}/C_{ISS} when selecting the low-side MOSFET. Adding a resistor between the BST and the C_{BST} can slow the high-side MOSFET turn-on. Similarly, adding a capacitor from the gate to the source of the high-side MOSFET has the same effect. However, both methods are at the expense of increasing the switching losses.

High-Speed, Dual-Phase Gate Driver for Multiphase, Step-Down Converters

Table 1. Typical Component Values (250kHz Operation, 20A/Phase Output Current)

COMPONENT	DESCRIPTION	PART NUMBER
C1	5 x 330µF/25V, 23mΩ (max) ESR input filtering capacitor	Sanyo 25MV330WX
C2	2.2µF/10V ceramic capacitor	Taiyo Yuden JMK107BJ225MA
C3, C4	0.22µF/10V ceramic capacitors	Taiyo Yuden GMK212BJ224MG
C5, C6	3 x 820µF/4V, 12mΩ (max) ESR electrolytic capacitors	Sanyo 4SP820M
C7	0.1µF/10V ceramic capacitor	Taiyo Yuden UMK212BJ104MG
D1	Dual Schottky diode	Central Semiconductor CMPSH-3A
L1, L2	0.66µH/29A, 2.1mΩ (typ), 2.5mΩ (max) R_{DC} inductors	Sumida CDEP134-H
Q1, Q2	High-side MOSFETs	Siliconix SUB70N03-09BP
Q3, Q4	Low-side MOSFETs	Fairchild FDB7045L
R1	10Ω ±5% resistor (0603)	V_{CC} decoupling resistor
R2	2kΩ to 125kΩ ±1% dead-time delay programming resistor (0603)	—

Table 2. Typical Component Values (800kHz Operation, 20A/Phase Output Current)

COMPONENT	DESCRIPTION	PART NUMBER
C1	5 x 10µF/25V, 10mΩ (max) ESR input filtering capacitor (1812)	Taiyo Yuden TMK432BJ106MM
C2	2.2µF/10V ceramic capacitor	Taiyo Yuden JMK107BJ225MA
C3, C4	0.22µF/10V ceramic capacitors	Taiyo Yuden GMK212BJ224MG
C5, C6	3 x 680µF/2V, 5mΩ (max) ESR SP capacitors	Sanyo 2RSTPD680M5
C7	0.1µF/10V ceramic capacitor	Taiyo Yuden UMK212BJ104MG
D1	Dual Schottky diode	Central Semiconductor CMPSH-3A
L1, L2	0.23µH/30A, 1.1mΩ (max) R_{DC} inductors	TDK SPM12535T-R23M300
Q1, Q2	High-side MOSFETs	IR IRF7801
Q3, Q4	Low-side MOSFETs	IR 2XIRF7822
R1	10Ω ±5% resistor (0603)	V_{CC} decoupling resistor
R2	2kΩ to 125kΩ ±1% dead-time delay programming resistor (0603)	—

High-Speed, Dual-Phase Gate Driver for Multiphase, Step-Down Converters

Applications Information

Power Dissipation

Power dissipation in the IC package comes mainly from switching the MOSFETs. Therefore, it is a function of both switching frequency and the total gate charge of the selected MOSFETs. The total power dissipation when both drivers are switching is given by:

$$P_{IC} = 2 \times f_S \times (N \times Q_{G\_TOTAL\_HS} \times \frac{R_{HS}}{R_{HS} + (R_{G\_HS} / N)} + M \times Q_{G\_TOTAL\_LS} \times \frac{R_{LS}}{R_{LS} + (R_{G\_LS} / M)}) \times V_{PV\_} + V_{VCC} \times I_{VCC}$$

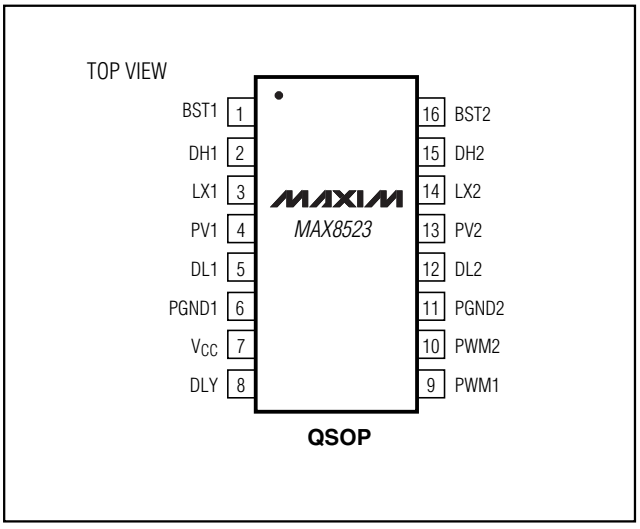
where f_S is the switching frequency, $Q_{G\_TOTAL\_HS}$ is the total gate charge of the selected high-side MOSFET, $Q_{G\_TOTAL\_LS}$ is the total gate charge of the selected low-side MOSFET, N is the total number of the high-side MOSFETs in parallel, M is the total number of the low-side MOSFETs in parallel, $V_{PV\_}$ is the voltage at the PV_ pin, R_{HS} is the on-resistance of the high-side driver, R_{LS} is the on-resistance of the low-side driver, R_{G_HS} is the gate resistance of the selected high-side MOSFET, R_{G_LS} is the gate resistance of the selected low-side MOSFETs, V_{VCC} is the voltage at the V_{CC} pin, and I_{VCC} is the supply current at the V_{CC} pin.

PC Board Layout Considerations

The MAX8523 MOSFET driver sources and sinks large currents to drive MOSFETs at high switching speeds. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following PC board layout guidelines are recommended when designing with the MAX8523:

1) Place all decoupling capacitors (C2, C3, C4, C7) as close to their respective pins as possible.
2) Minimize the high-current loops from the input capacitor, upper-switching MOSFET, and low-side MOSFET back to the input capacitor negative terminal.
3) Provide enough copper area at and around the switching MOSFETs and inductors to aid in thermal dissipation.
4) Connect the PGND1 and PGND2 pins of the MAX8523 as close as possible to the source of the low-side MOSFETs.
5) Keep LX1 and LX2 away from sensitive analog components and nodes. Place the IC and analog components on the opposite side of the board from the power-switching node if possible.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 1187

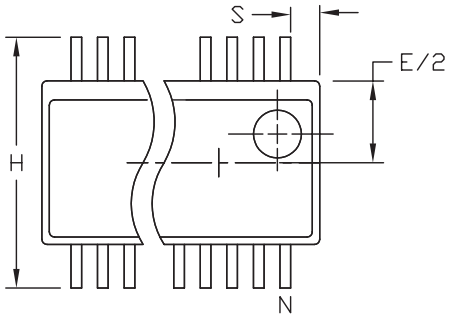
PROCESS: BiCMOS

High-Speed, Dual-Phase Gate Driver for Multiphase, Step-Down Converters

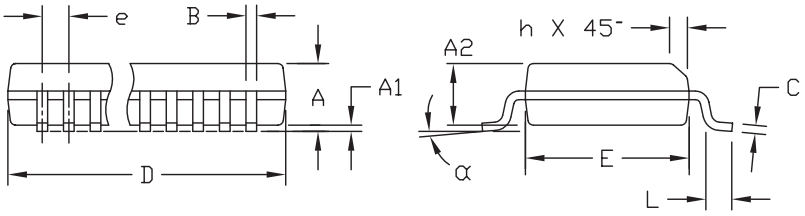
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	D	1/1